Attorney Docket No. 10559-391001
Serial No.: 09/745,104
Amendment dated January 20, 2004
Reply to Office Action dated November 19, 2003

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

The title of the invention stands objected to as not being descriptive. In response, the title is changed to "Hardware Loops and A Pipeline System Using Advanced Generation of Loop Parameters". However, should the Examiner have any suggestions for a title which is more descriptive, these suggestions would be appreciated.

The entire specification has been reviewed, and a few minor typographical errors are corrected.

Claims 1-18 and 20-25 stand rejected under 35 USC 102 as allegedly being anticipated by Atkins. This contention is respectfully traversed. However the claims are amended to better emphasize their patentable distinctions.

First, Atkins does in fact show a pipelined system, and as part of this system, includes extensive descriptions of maintaining memory contents within the cache. Atkins also teaches instructions for setting up the loop, described as the SET LOOP instruction at column 2, line 28.

As described in Atkins, and in the background of the present specification, one main problem is that these loops may

take several hardware cycles to set up. For example, page 9, lines 14-20 of the present specification describes that a loop set up penalty is caused because the system stalls the pipeline until the data is available. Atkins includes an analogous problem; as explained at column 8, beginning at line 40, multiple cycles are taken in order to form the instruction, (instruction decode; column 8, lines 40-41) then in the next cycle, getting the effective address portions (lines 46-47); then a third cycle (line 51) accessing the data. Finally, the result is written into the general-purpose registers, and then sent to the execution unit; see column 9, line 8.

The SET LOOP hardware is operated in a similar way. See generally, column 9, line 13 through column 10, line 55. The parameters for the loop are calculated, and used to load the loop and execute the loop in Atkins.

In order to emphasize the patentable distinctions over Atkins, claim 1 has been amended to include the limitations of claim 3 therein, and also to define that the conditions for the hardware loop are defined within a program and then used in two different pipelines to propagate two different conditions. Simultaneously, as described above, Atkins does not teach or suggest this feature, and therefore it is respectfully suggested that claim 1 is patentable thereover. Claim 1 enables the two

conditions to be executed in two different pipelines simultaneously, thereby reducing the loop penalty.

Claim 2 has also been amended to define additional aspects whereby the registers are used to begin calculating parameters based on those loop conditions prior to the propagate. In this way, the loop hardware begins to operate before the calculations are complete. This is not taught or suggested by Atkins. The description of the set loop hardware beginning at column 9, line 13 teaches nothing about calculating parameters prior to the propagation of the loop parameters. Therefore, claim 2 is even further allowable thereover.

Claim 7 has been amended to include similar limitations therein to those discussed above with respect to claim 2. Specifically, claim 7 has been amended to recite that the loop values are calculated prior to the propagating, to avoid the setup penalty discussed above. Claim 10 includes similar limitations to those discussed above in claim 1, and should be allowable for similar reasons to those discussed above.

Claim 13 has been amended in a similar way to claim 1 and should be allowable for similar reasons.

Claim 22 has been amended in a similar way to claim 7 and should also be allowable for similar reasons.

Claims 26 and 28 have also been amended in similar ways to those discussed above, and each should, hence, be allowable.

Claim 19 was rejected over Atkins in view of Tran. While Tran does in fact teach the use of speculative registers, he teaches nothing about using those speculative registers in order to begin a loop hardware operation prior to propagation of parameters, as now claimed. Therefore, claim 19 should be additionally allowable on its own merits.

In view of the above amendments and remarks, therefore, all the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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